		Document:	Page: 1 of 14
	Galleon Embedded Computing	GEC-WP-1403	1 01 14
galleon		Revision:	Date:
embedded computing	Whitepaper	1.5	4-Sep-17
Title: Solid State Storage			

Solid State Storage in Military and Aerospace Applications

Revision history:

Rev.	Date	Changes	Sign
1.0	28-Mar-14	Document created	EB
1.1	24-May-14	Minor updates and grammatical corrections	EB
1.2	30-Jan-15	Updated MLC capacity	EB
1.3		Updated MLC and SLC capacity and P/E numbers	CG
	07-Jul-16	Updated footer notes	HT
1.4	24-Apr-17	Updates for capacity updates and for eMLC	HT
1.5	4-Sep-17	Updates with latest flash data	HT

Abstract

This document describes the different types of Solid State Storage available on the market today. The types are evaluated from a technical and commercial standpoint with respect to the relevance for their use in military and aerospace applications. The most important benefits and concerns with the different storage technologies are discussed.

		Document:	Page:
	Galleon Embedded Computing	GEC-WP-1403	2 of 14
galleon		Revision:	Date:
embedded computing	Whitepaper	1.5	4-Sep-17
Title: Solid State Storage		•	·

1 FLASH based Solid State Storage

1.1 Introduction

There are currently 2 main types of FLASH memory used in solid state storage devices: Multi-Level Cell (MLC) and Single Level Cell (SLC). The SLC technology stores a single data bit per memory cell. The Multi-Level Cell technology stores data by programming a memory cell with two or more bits by altering the programming level of the cell. Hence, a two-bit cell can be visualized as follows:

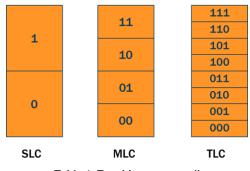


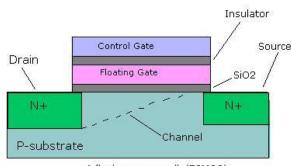
Table 1, Two-bit memory cell.

MLC technology is evolving very quickly, and there are several variants on the market. Tri-level (TLC) and Enterprise MLC (eMLC) are two such derivatives. There are also newer variants based on 3D memory cells, but these are not available in rugged variants yet, at least not with sufficient reliability over full temperature range as to be useful for this market.

1.2 SSD memory limitations

SSDs (Solid State Devices) all use Flash memory of some sort. All flash memory has inherent limitations due to the design of the storage cell (shown below).

		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 3 of 14
	galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			



A flash memory cell (FGMOS)

The process of programming the cell involves storing charge from the floating gate, with electrons tunneling through the SiO2 layer. Erasing the cell involves removing the charge. Reading the cell involves passing a current through the substrate, and detecting the effect of the stored charge (or not) in the process. MLC works by varying the amount of charge storage, so that 4 separate states can be detected, and TLC works similarly with 8 levels of charge.

With NAND flash, all cells in a block are erased together, and cells are programmed individually. The block erase function is because the cells in the blocks are very close together on the silicon, and it's impossible to erase one cell without having some impact on the adjacent cell.

1.2.1 Data retention

Once the charge is stored, it will gradually dissipate, and eventually it will get to the point that it is read with the wrong state. Read cycles accelerate that dissipation. For a healthy flash cell, this loss of state takes a very long time (many years for single layer cell, SLC, flash).

For most applications, data retention of a healthy flash cell is not an issue.

1.2.2 Wear out

The act of programming the cell degrades it slightly each time. This degradation of the cell has 2 effects:

- It can impact the ability of the cell to be programmed/erased correctly (i.e. it is stuck at one value).
- Data retention is reduced for flash cells which have been written many times.

1.2.3 Temperature effects

As with most electronics, temperature has a negative effect on the flash memory limitations.

Low temperatures are particularly bad for wear-out effect on the ability to program the device, and high temperatures are particularly bad for data retention.

		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 4 of 14
	galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			

Different flash technologies, and even different flash chips differ in their level of survival at high and low temperatures.

1.2.4 Wear out is not the same as unreliability

An important note related to flash wear out is that it is not the same as unreliability.

SSDs are extremely reliable, with MTBF figures being in the range 1-3million hours.

Wear out doesn't relate to the number of hours that the flash memory has been used (MTBF). Instead, it is related to the number of program/erase cycles which are applied to the flash memory. i.e. it is the type of usage that it is put to which counts.

Wear-out is an extremely predictable behavior, and if handled by user application (see section 1.3.4 below), will not lead to any errors occurring in the system/application.

In contrast, failures estimated with MTBF predictions, are non-predictable, and cannot be mitigated without higher level solutions (e.g. dual or triple redundant techniques).

1.3 SSD wear out mitigation techniques

Different flash memory technologies have differing abilities to mitigate flash memory wear out.

1.3.1 Bad block detection

Rugged SSDs implement ECC (Error Checking and Correcting) algorithms on the data, so that they can detect bit errors in the data, and also detect that a block of the flash memory is near the end of its useable life. The ECC functionality will be used on each block read cycle, with the capability of correcting, for example, >50 error bits in each block (typically 512 or 1024 bytes). By correcting these errors, the SSD can ensure that the user application sees the correct data, even though the block is starting to deteriorate.

Once a block is detected as having any errors, it is not used any longer.

1.3.2 Spare Capacity

To ensure that the available memory space remains the same, when the SSD detects bad blocks, the SSDs provide spare capacity. So, when a block is detected as bad, more memory space is made available, to ensure that the user accessible address space remains the same.

1.3.3 Wear levelling

Deterioration of the flash cells is most heavily affected by each program/erase (P/E) cycle. Therefore, the SSD controller will spread the programming of data around its available memory space, while maintaining an address translation table to ensure that the data is still accessible at the same bus address as previously.

		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 5 of 14
	galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			

Using this technique hugely increases the life for an SSD, especially in server type applications where a large number of random write cycles may be occurring in a small address space.

For data recording application, wear levelling is less useful, but still helps when the normal recorded data is less than would fill the SSD.

1.3.4 SMART monitoring

The SSDs provide a set of registers which can be accessed over their connected bus (e.g. SATA) to provide information on the status of the device.

This varies by the SSD vendor, but typically includes a wear-out indicator. This tells the user application whether the SSD is close to the end of its life.

The wear-out indicator is based on a few different factors (e.g. number of P/E cycles applied, number of bad blocks detected, etc.), and can differ for each SSD vendor. But in all cases, this indication can be used by the system to detect when the SSD should be replaced, to ensure that no errors will occur (which can't be handled by the ECC algorithm).

1.3.5 TBW vs P/E cycles

With the host of mitigation functions available within the SSDs, the market operates with 2 different measures for longevity.

The Program/Erase cycle count relates to the flash cell, as described above.

In addition, a figure called TBW, or Total Bytes Written, is used to estimate the actual longevity of the device. TBW figures vary hugely based on the underlying flash technology, the flash silicon design, and the spare capacity (and other mitigation techniques described above).

NB TBW figures are often quoted for sequential write cycles of the entire device (i.e. 1 P/E cycle per block per complete block being written). This is basically the same as the number of P/E cycles for the flash memory blocks, expanded by a little for the spare capacity. For recording applications, that is valid, but for most server type applications it can be a bit misleading. For a typical computing type application, the TBW number could be around one half to one third of the TBW figure for sequential applications.

1.4 Types of SSD

1.4.1 SLC Memory

SLC (Single-Level Cell) memory is primarily used in Military applications. Since only a single bit is stored per memory cell, SLC technology offers low data density compared to other memory technologies. The main benefit of SLC technology is very high reliability due to the robustness of the single bit programming. Many SLC SSDs are guaranteed for over 60 000 program-erase

	Galleon Embedded Computing	Document: GEC-WP-1403	Page: 6 of 14
galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title: Solid State Storage			

cycles and very long data retention periods (often >10 years). Some vendors also offer extremely wide temperature range (-50°C to +115°C) and even space qualified SSDs.

Due to the relatively low-volume market (compared to MLC technology which is also used in the commercial market), SLC technology is typically lagging by one or two generations compared to MLC technology. Until a few years ago, SLC was outperforming MLC based SSDs on write performance due to more efficient programming of single level cells. This is no longer the case due to previous generation controllers typically used on SLC SSDs in combination with higher capacity MLC based SSDs typically having an internal architecture with multiple memory banks allowing for parallel access to the memory cells for increased performance.

Due to low volume, low capacity and very specialized designs, the SLC based SSDs are significantly higher cost per gigabyte compared to any other storage technology. Prices are relatively stable and do not show the downward trend experienced in other memory technologies.

TBW figures or SLC SSDs are often in the range 50-100 thousand times the size of the SSD.

1.4.2 MLC Memory

MLC (Multi-Level Cell) flash memory involves storing more than 1 data bit on each NAND flash cell. This provides a four-fold increase in the memory density, when compared to SLC memory. The actual memory density difference is more than that because the MLC market size has driven MLC technology forward.

MLC based memory is now the most commonly used throughout the industry, both for commercial and industrial applications. Due to the multi-bit per cell technology, it is possible to create much higher memory densities using MLC technology compared to SLC. A lot of effort is put into developing ever increasing capacities and higher performance SSDs by the vendors in this market segment. The technology drive is pushed by the exponentially increasing storage demand in the consumer and professional markets. The technology follows Moore's law with capacities doubling every 12-18 months while prices are cut in half at approximately the same rate for commercial grade parts.

The demand for increased capacity and performance also in the industrial and military markets have resulted in a wide offering of MLC SSDs supporting extended temperatures and rugged environments. Although MLC technology by nature is less robust than SLC technology, the rapid development of MLC FLASH controllers has mitigated much of this concern. Both controllers and FLASH is offered as full industrial grade components. Serious vendors of MLC based industrial SSDs now offer very reliable SSDs with extended temperature range, -40°C to +85°C, conformal coating, and mechanically stabilized designs.

Due to better controllers and parallelized designs, the performance of the MLC based SSDs now outperform the SLC technology. Sustained write speeds greater than 500MB/s with 6 Gbit SATA 3 interfaces are common.

Galleon Embedded Computing, Proprietary and Confidential. This document contains proprietary information. It is provided with the understanding that the document will not be shared outside of the Company that it is sent to.

		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 7 of 14
	galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			

The combination of excellent performance, high capacity, good reliability and competitive pricing makes MLC based SSDs an attractive alternative for many military and industrial applications.

MLC technology is more susceptible to memory cell wear-out than SLC technology. Rugged (industrial grade) MLC based SSDs provide TBW numbers of between 1 000 to 5 000 times the size of the SSD.

1.4.3 eMLC Memory

The term "Enterprise MLC" (or sometimes referred to as "Enhanced MLC") is used for SSDs targeted for high endurance applications such as use in data center and high-performance servers. eMLC is enhanced technology to mitigate the write endurance issues encountered with standard MLCs. By enhancements to the memory cells, the number of guaranteed programerase cycles is increased to 20 000 to 30 000 cycles, thus improving write endurance by a factor of 5-10 compared to standard MLC technology.

Due to the improved write endurance, eMLC is commonly used in enterprise server applications (hence the name), where 24/7 operation is required.

eMLC is currently only marketed for the 0 to +70°C temperature range, as this is what is required for enterprise environments. Some vendors still use industrial grade components in their designs.

eMLC drives at extended temperatures

Galleon Embedded Computing have performed extensive testing on eMLC drives from several manufacturers, and have found that it is possible to select devices which will pass functional and performance tests at room temperature.

However, the testing has also proven that eMLC drives wear out is much worse than standard MLC when at low/high temperatures. i.e. the key advantage of eMLC is lost when the drive is stored or operated at low or high temperatures.

Because of this testing, Galleon no longer offers eMLC drives for our rugged recording products, where high temperature operation is typically required.

			Document:	Page: 8 of 14
		Galleon Embedded Computing	GEC-WP-1403	0 01 14
	- galleon	Calleon Embedded Computing	Revision:	Date:
	embedded computing	Whitepaper	1.5	4-Sep-17
Title:	Solid State Storage		•	·

2 SSD Comparison Summary

The below table lists key parameters for the various SSDs discussed in the previous sections.

Parameter	Commercial Grade MLC	Industrial Grade MLC	Military Grade SLC
FLASH Technology	MLC	MLC	SLC
Max Capacity*	4TB	20TB	2TB
Temperature range**	0 to +50°C	-40°C to +85°C	-55°C to +115°C
Write endurance (P/E cycles)	75-500	1K-5K	60-150K
Secure Erase***	no	yes	yes
Conformal Coating Options	no	yes	yes

Table 2, SSD Comparison Chart.

- * Available per July 2017
- ** As specified by factory reported on individual drive level
- *** On select models only

		Document:	Page:
	Galleon Embedded Computing	GEC-WP-1403	9 of 14
galleon		Revision:	Date:
embedded computing	Whitepaper	1.5	4-Sep-17
Title: Solid State Storage		·	

3 Write Endurance Considerations

In some cases, the write endurance characteristics of MLC SSDs are a concern. The average daily program-erase cycles experienced by a memory cell are highly dependent on the application and usage model. Let's consider two example scenarios:

- a) A mission data recorder is used to store video captured in-flight. The capacity of the storage media is equivalent to the amount of data captured during the flight. In this case, data is sequentially written to the storage media until the media is full, and/or the flight is complete. After the flight, the data is copied to ground based storage and the storage media is erased and prepared for the next flight. Each flight represents a single write-erase cycle. The entire capacity is written once, and read once, per flight. Due to over-provisioning, the full capacity write only writes to 85-90% of the actual memory cell capacity. Assuming the storage media is used for one flight per day, 365 days per year, the media will wear out after 5-10 years. SLC based SSDs on the other hand would last over 100 years if used in this application! Note that we are considering write endurance only in this example, and not taking other factors like temperature variations, humidity, vibration, etc, into account.
- b) Let us now consider an instrumentation recorder which is used to record experiments of some sort. The recorded data will continuously be written to the storage media until a trigger stops the recording. The storage media is used as a ring-buffer, and will start over from the beginning immediately when the full capacity is reached. Each full capacity write represents a program-erase cycle. Contrary to scenario a) above, the media will be programmed and erased multiple times during each experiment. Assuming the data rates are such that the media is filled once per 30 minutes of recording, a 24-hour experiment will be equivalent to 48 program-erase cycles. If used 8 hours per day every day (including weekends), the media will be worn out in less than six months when using standard MLC SSDs. However, if SLC based SSDs were used, the usable timeframe would be extended to 15 years or more with this usage pattern.

Consequently, the selection of storage media type is highly dependent on the usage model being applied.

There are, however, other factors which might further complicate the picture. Let us assume scenario b) above one more time:

Let us also assume that we use MLC technology SSDs. Given the example above, the media would wear out in 6 months in this case, given a certain storage capacity and average data rate. Now, if we could double the capacity of the SSD, the time to fill the entire capacity would be twice as long, and consequently the time to wear out the media would increase from 6 months to 1 year, everything else being equal. Note that the same also applies to a), since only ½ the capacity of the media would be used per flight. Using higher capacity storage media than what is strictly required could be cost effective in use-cases where media wear-out is a concern.

		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 10 of 14
	galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			

Note that write endurance (and data retention) is adversely affected by low and high temperatures. This negative effect of high temperature on wear out is much greater with eMLC drives than with MLC or with SLC drives (as mentioned in section 0 above).

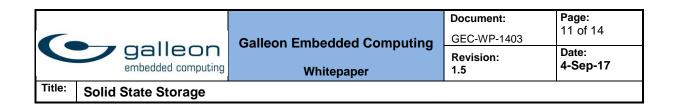
3.1 Recorder application

With the Galleon data recorders and servers, the main storage memory is removable.

If this removable memory is easily accessible on whichever platform it is installed on, this can have a huge effect on the choice of memory technology for the application.

By using the SMART monitoring tools mentioned above in 1.3.4, the user application can easily detect when an SSD is nearing the end of its useful life, and can flag that it would need to be replaced at the next 1st level maintenance cycle. In many cases, this allows the easy use of MLC technology where SLC would perhaps have been used in the past.

With memory capacity per \$ much higher with MLC than with SLC, MLC will often work well in high reliability applications, with the memory being replaced at standard maintenance cycles.



4 Galleon SSD Offerings

Galleon offers the full range of solid state storage media, from commercial grade MLC to military grade SLC. The offerings are continually monitored and updated as required, when old SSDs go obsolete and new variants enter the market. The Galleon product is based on combining multiple SSDs into a single Removable Data Module (RDM).

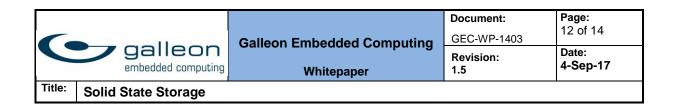
Galleon RDM P/N	Туре	RDM Capacity	Operating temp range*	Comments
XSR-RDM-xxxxC-yyy	MLC	1TB, 2TB, 4TB	0°C to +35°C	Low cost. Very high performance. Commercial grade, MLC. Not conformal coated.
XSR-RDM-xxxxL-yyy	MLC	1TB, 2TB, 4TB, 8TB	-40°C to +71°C	Good performance. Industrial grade, MLC. Conformal coating. Excellent price/performance ratio.
XSR-RDM-xxxxN-yyy	MLC	1TB, 2TB, 4TB, 8TB, 16TB, 20TB, 40TB	-40°C to +71°C	Good performance. Industrial grade, MLC. Conformal coating. Good price/performance ratio. Very high capacity. US Manufacturer
XSR-RDM-xxxxS-yyy	SLC	1TB, 2TB, 4TB, 8TB	-50°C to +75°C	Extremely high endurance. Good performance. Military grade, SLC. Conformal coating.
			Calloon SSD Offering	Highest cost.

Table 3, Galleon SSD Offerings.

xxxx Unformatted drive capacity in GB (i.e. 1000 = 1TB)

yyy Revision/type code

Operating temperature when installed in the Galleon XSR recorder/server



5 Lifecycle Management Considerations

Due to the very rapid development in the Solid-State Storage market, classic lifecycle management with 10-15 years' scope is not feasible for SSDs, with the possible exception of military grade SLC devices where vendors try to extend the lifecycles of the offered products by stocking FLASH chips and controllers to support existing programs.

Galleon continuously monitor the SSD market space and add new SSD options as they become available. Simultaneously, it is necessary to phase out parts which are announced End of Life (EOL), or simply become unavailable in the market. The latter is typically the case for commercial grade SSDs which are discontinued by the vendors with no notice.

In such cases, Galleon strives to offer functionally (FFF) equivalent products with equal or better performance on all relevant parameters compared to the discontinued product.

Before a new SSD vendor or part is offered as part of Galleon's product offering, the SSD undergoes extensive test and qualification in Galleons laboratories validating drive build quality, component selection, performance, etc, as well as thorough scrutiny of the vendors' quality management system, previous delivery performance, and so on.

galleon embedded computing		Galleon Embedded Computing	Document: GEC-WP-1403	Page: 13 of 14
			Revision: 1.5	Date: 4-Sep-17
Title:	Solid State Storage			

6 Questions or Comments

This whitepaper will be updated on a regular basis as SSD technology evolves.

Any questions or comments to the contents are welcome and appreciated. Please contact Hugh Tarver, at <u>htarver@galleonec.com</u> or send your feedback to <u>info@galleonec.com</u>

	Galleon Embedded Computing	Document: GEC-WP-1403	Page: 14 of 14
galleon embedded computing		Revision: 1.5	Date: 4-Sep-17
Title: Solid State Storage			

7 References

Web article "Industrial Temperature and NAND Flash in SSD Products", Eli Tiomkin, Western Digital, 24.07.2012, <u>http://www.eeweb.com/blog/eli_tiomkin/industrial-temperature-and-nand-flash-in-ssd-products</u>

Web article "**SLC vs MLC: Which works best for high-reliability applications?**", Charlie Cassidy, Tele Communication Systems, 16.07.2012, <u>http://www.eetimes.com/document.asp?doc_id=1279762</u>